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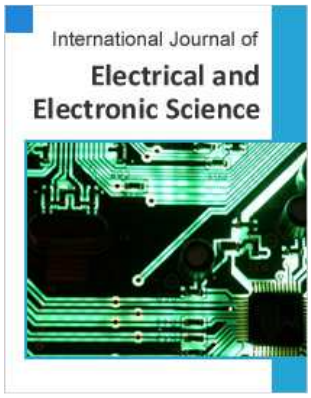

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AC-DC Converter with Constant Current Output CMOS IC Design Based on DCM Fly-Back Topology

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Abstract

Fly-back topology is widely used in AC-DC converter design for its many irreplaceable outstanding characteristics over the other isolated topologies. In the previous AC-DC converter solution, usually, an opto-coupler is added on secondary feedback circuitry for transforming the output signal into light and then achieving feedback control without directly connected to primary-side circuitry. If taking the system cost and PCB volume into consideration, it is better to replace the expensive opto-coupler with a transformer which has another auxiliary winding for detecting output signal except primary and secondary winding. Unfortunately, the forward-biasing voltage drop on the essential rectifier diode and power lost on auxiliary winding make the foregoing auxiliary winding solution with lower accuracy and efficiency. For a balance between cost and accuracy, an AC-DC converter with zero-cross detection (ZCD) is proposed in this paper. Control principle analysis and comparison on accuracy, efficiency and cost between the three different solutions are given in this paper for brief summarizing AC-DC converter with constant current output CMOS IC design based on discontinuous conduction mode (DCM) fly-back topology.

1. Introduction

AC-DC switching power supply management converter CMOS IC is widely used in many kinds of electronic equipment, such as power adapter and charger for mobile phone, PC, MP3/MP4, etc. AC-DC switching power supply can stable the output voltage or current by controlling the frequency of switch (PFM) and duty cycle (PWM) using modern power electronic technology There are many researches focus on low-power efficiency, output precision and anti-interference for AC-DC converter [1, 2].

Constant current is ubiquitous on electronic applications, like LED driver and lithium battery charger. Light Emitting Diode (LED) is widely used in vehicles and traffic lights, house and street lighting, commercial signs and so on. By concerning its outstanding characteristics, like high theoretical luminous efficacy, long lifetime, environmentally friendly, chromatic variety, LED will be the trend in lighting. However, for boosting and taking advantage the aforementioned advantages, LED usually need power supply topology with constant current driver especially designed for them. In the previous solution, LED driver uses photoelectric couple in secondary-side feedback circuitry or auxiliary winding in primary-side feedback circuitry to detect load condition and achieve feedback control. Inevitability, it reduces the effect of isolation which has been widely used in LED driver for safety and both raises the manufacturing cost accordingly [3, 4].

For safety, isolation is required ubiquity in state-of-the-art AC-DC converter design.

Potentially lethal transient voltages and currents on primary-side can be prevented by isolated converter design, like fly-back topology. Fly-back topology is widely used in AC-DC converter design for its many irreplaceable outstanding characteristics over the other isolated topologies. Many topologies require a separate inductor acted as power storage. This inductor can be eliminated in fly-back topology for in reality the fly-back transformer is storage inductor. Coupled with this fact that the rest of circuitry is simple, fly-back topology is a cost effective and popular topology for AC-DC converter design.

In the previous AC-DC converter design solutions based on fly-back topology, usually, an opto-coupler is added on secondary feedback circuitry for transforming the output signal into light and then achieving feedback control without directly connected to primary-side circuitry. Opto-coupler cans response fast for a higher accuracy. However, obviously, opto-coupler is more expensive than other components and increases the system cost. And also, the use of photoelectric coupler and precision voltage source cased insecurity isolation between primary-side and secondary-side [5-8]. If taking the system cost and PCB volume into consideration, it is better to replace the expensive opto-coupler with a transformer which has another auxiliary winding for detecting output signal except primary and secondary winding [9-12]. Unfortunately, the forward-biasing voltage drop on the essential rectifier diode and power lost on auxiliary winding make the foregoing auxiliary winding feedback solution with lower output current accuracy and system efficiency. For a balance between cost and accuracy, an AC-DC converter with zero-cross detection (ZCD) is proposed in this paper. Control principle analysis and compare on accuracy, efficiency and cost between the three different solutions are given in this paper for summarizing AC-DC converter with constant current output CMOS IC design based on discontinuous conduction mode (DCM) fly-back topology [13-15].

2. DCM Fly-Back Topology

The fly-back topology is isolated by using transformer which has primary winding and secondary winding with opposite polarity, as the power storage inductor. By varying the secondary winding turns, the output voltage or current can be adjusted and also multiple outputs are possible with different secondary winding. Especially, in low-power applications, the fly-back topology is the simplest and most common isolated topology.

As depicted in Fig.1, the RCD snubber network on the primary side is to clamp the drain voltage of switching NMOS. The leakage inductance can be seen as part of the energy stored in the transformer that will not be transferred on the secondary and to the load. This energy need to be dissipated in the primary side through an external snubber. When the power MOSFET is turned off, there is a high voltage spike on the drain due to the transformer leakage inductance. This excessive voltage on the MOSFET may lead to an avalanche breakdown and eventually failure of the device. Therefore, it is necessary to use an additional network to clamp the voltage. The RCD snubber network absorbs the current in the leakage inductance by turning on the snubber diode once the MOSFET drain voltage exceeds specified value.

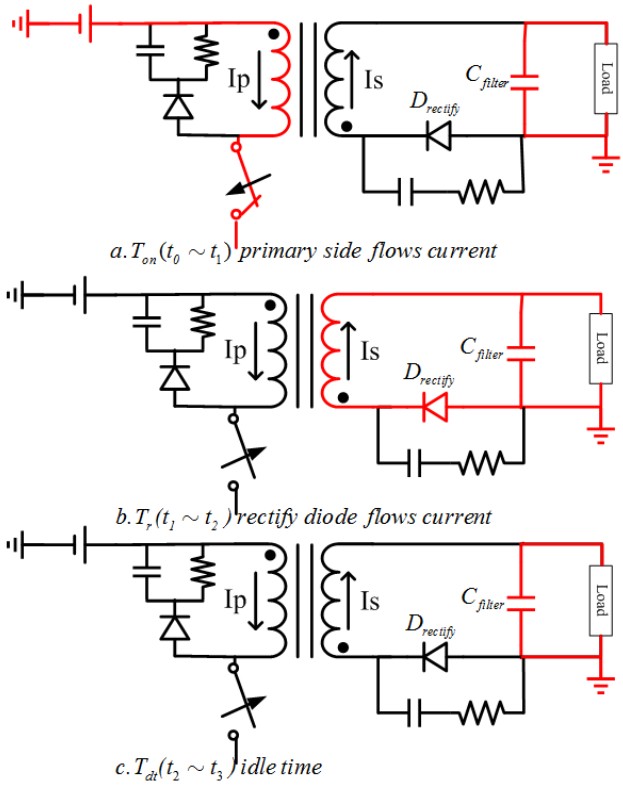

Fig. 1. *Three operation states about DCM fly-back topology.*

There are three different operation states in discontinuous conduction mode (DCM) fly-back topology. As depicted in Fig.1 (a), when primary-side switch turns on, except bridge diodes for input voltage AC to DC converting, all rectifier diodes become reverse-biased, and all output load currents are supplied from the output filter capacitors. During this ON time, input voltage is applied across the primary-side winding, and primary-side conduction current increases linearly from zero to the peak value with a slope Vin/Lp. Actually, the transformer acts like a pure inductor. In Fig.1 (b), when primary-side switch turns off, all winding voltages reverse under fly-back action, bringing the output diode into conduction and the power stored on primary winding is delivered to the secondary-side and decomposed into supply load current and replenish the charges on the output filter capacitor. When the secondary winding conducts, the output voltage, together with rectifier diode forward biasing voltage drop, are applied across the secondary winding and secondary winding current decreases linearly from the peak value to zero with a slope (Vo-Vdiode)/Ls. In Fig.1 (c), after secondary winding current drops to zero, the primary-side switch doesn't turn on immediately. All the energy stored in the primary during the on time is completely delivered to the secondary

and to the load before the next cycle, and there is also a dead time between the instant the secondary current reaches zero and the start of the next cycle. In the continuous mode there is still some energy left in the secondary at the beginning of the next cycle. This mode is called discontinuous conduction mode (DCM).

During ON time, the power is stored on primary winding can be expressed as

$$P_{ON} = \frac{1}{2} L_P \cdot I_{ppk}^2 \quad (1)$$

Where L_P is the primary winding inductance and I_{ppk} is the primary-side peak current at the end of ON time.

The primary-side to secondary-side ampere-turns ratios is conserved for energy conservation. So the secondary winding peak current can be given by

$$I_{spk} = \frac{N_p}{N_s} \cdot I_{ppk} \quad (2)$$

Where N_p and N_s is the number of primary winding turns and secondary winding turns accordingly.

3. SSR with Opto-Coupler Isolation

In electronics, an opto-coupler also called an opto-isolator is a component that transfers electrical signals between two isolated circuits by using light. Opto-coupler prevents high voltages from affecting the system receiving the signal and better application safety for customer.

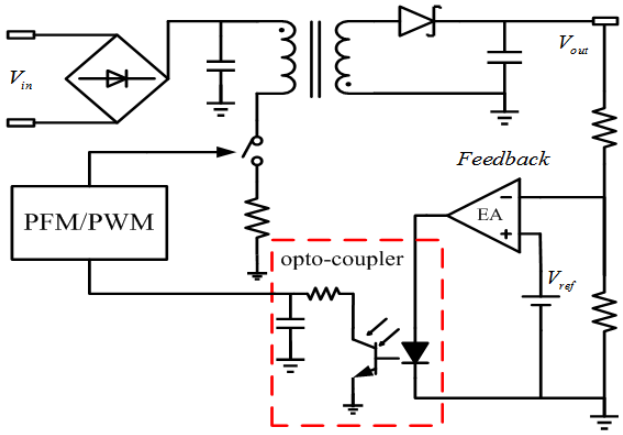

Fig. 2. *SSR with opto-coupler isolation.*

As depicted in Fig.2, the opto-coupler on the secondary-side detects the output voltage by resistors sampling network. Combining with precious voltage source, the difference between the feedback voltage and reference can be amplified by the Error-Amplifier. The light signal is converted into electronic signal on primary-side by opto-coupler and influence the following pulse-width modulation (PWM) and pulse-frequency modulation (PFM) control circuitry.

There are some advantages for using opto-coupler. First, the feedback circuitry, like Error-Amplifier and divided resistors sampling network, can be placed on the secondary-side. Under this reason, it is also called secondary-side regulation (SSR) converter. It is an irreplaceable preponderant characteristic for the output voltage can be directly sensed and regulated and with faster response. As a result, an elaborated SSR with opto-coupler can be expected with 1% to 3% accuracy overall operating input voltage, load current, and temperature conditions. Because of opto-coupler high precision and fast response, this method is widely used in previous solution.

However, if the size of the driver converter is strictly limited, the arrangement of the isolated opto-coupler in the layout of the PCB becomes a major problem. Also, the use of photoelectric coupler and precision voltage source cased insecurity isolation between primary side and secondary side. There's one more problem that for this area offers a large parasitic capacitance, an opto-coupler introduces an extra pole in the control loop, which reduces the converter's bandwidth and more hard to compensate the control loop.

4. PSR with Auxiliary Winding

If taking the system cost and PCB volume into consideration, there is an alternative solution to replace the expensive and larger volume opto-coupler with a transformer which has another auxiliary winding for detecting output load condition except primary and secondary winding.

A. Principle analysis

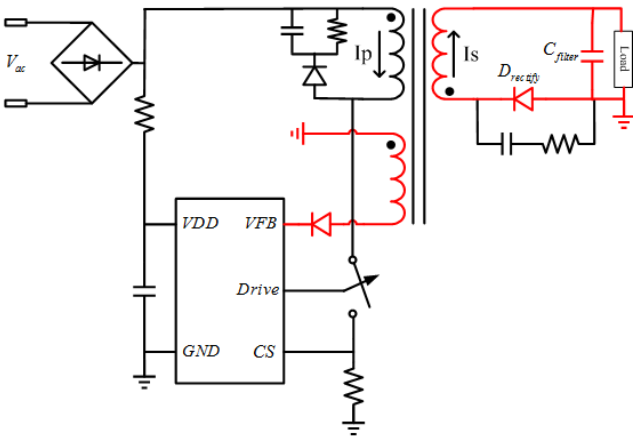

Fig. 3. *PSR with auxiliary winding.*

For detecting the output load condition, an auxiliary is added on the fly-back transformer. Now, the feedback circuitry can be placed on primary-side. So this solution is called primary-side regulation (PSR). In the schematic depicted on Fig.3, the auxiliary winding can offer the following features:

1. Supply power for the chip;
2. Detect the output load condition when secondary winding conducts current;
3. Detect the ring signal when the secondary winding current drops to zero;

4. Turn off the chip when the current or voltage in the system gets over large unexpectedly.

The power stored in the primary-side winding will be transformed to secondary-side and auxiliary-side when primary-side switch turns off. According to the fly-back ampere-turns ratio conservation

$$I_{ppk}N_p = I_{spk}N_s + I_{apk}N_a \tag{3}$$

The inductance is proportional to the square of number of windings turns, $L = L_0N^2$, and $P = 0.5I^2L$. In this proposed design, $N_p = 160$, $N_s = 12$ and $N_a = 42$. By calculating, it has $P_{auxiliary} = 2\%P_{secondary}$. So the Eq.3 can be simplified by

$$I_{ppk}N_p = I_{spk}N_s \tag{4}$$

During ON time, the power stored in primary-side is

$$P_{in} = \frac{1}{2}L_pI_{ppk}^2 / T \tag{5}$$

And $P_{out} = V_oI_o$, if $P_{out} = \eta P_{in}$, Where η (eta) is the power transform efficiency. Combing the above equations, the output current can be expressed by,

$$I_o = \frac{\eta L_p}{2} \cdot I_{ppk}^{\ 2} \cdot \frac{f}{V_o} \tag{6}$$

Based on the assumption that efficiency eta and primary inductance is constant during operation, if we want to get a constant output current, the primary peak current value and the ratio of frequency to output voltage should be regulated.

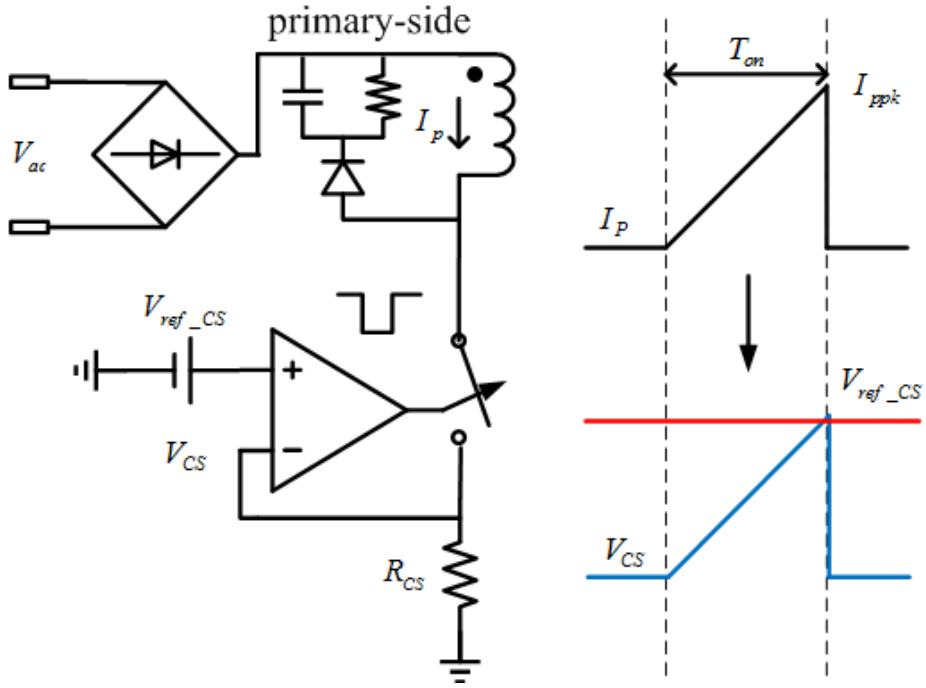

Fig. 4. *Current sense for regulating primary peak current value.*

B. Regulate primary peak current value

When primary-side switch turns on, input voltage is applied across the primary-side winding, and primary-side current increases linearly from zero to the peak value. Actually, the transformer acts like a pure inductor.

The primary peak current value can be given by,

$$I_{ppk} = \frac{V_{in}}{L_p} \cdot T_{ON} \tag{7}$$

The primary peak current value I_{ppk} can be specified by Current Sense circuit which is depicted in the Fig.4. When primary current I_P reaches to specified peak value I_{ppk} during ON time, current sense voltage V_{CS} across sampling resistor R_{CS} will rise to reference voltage V_{ref_CS}. At the same time, voltage comparator shut down primary-side switch.

And primary peak current value is set by

$$I_{ppk} = \frac{V_{ref\_CS}}{R_{CS}} \tag{8}$$

And also the secondary-side peak current can also be set by

$$I_{spk} = \frac{N_P}{N_S} \cdot \frac{V_{ref\_CS}}{R_{CS}} \tag{9}$$

C. Regulate the ratio of frequency to output voltage

For regulating the ratio of frequency to output voltage, voltage control oscillator should be used. A voltage control oscillator (VCO), as depicted in Fig.5, is an electronic oscillator whose oscillation frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency.

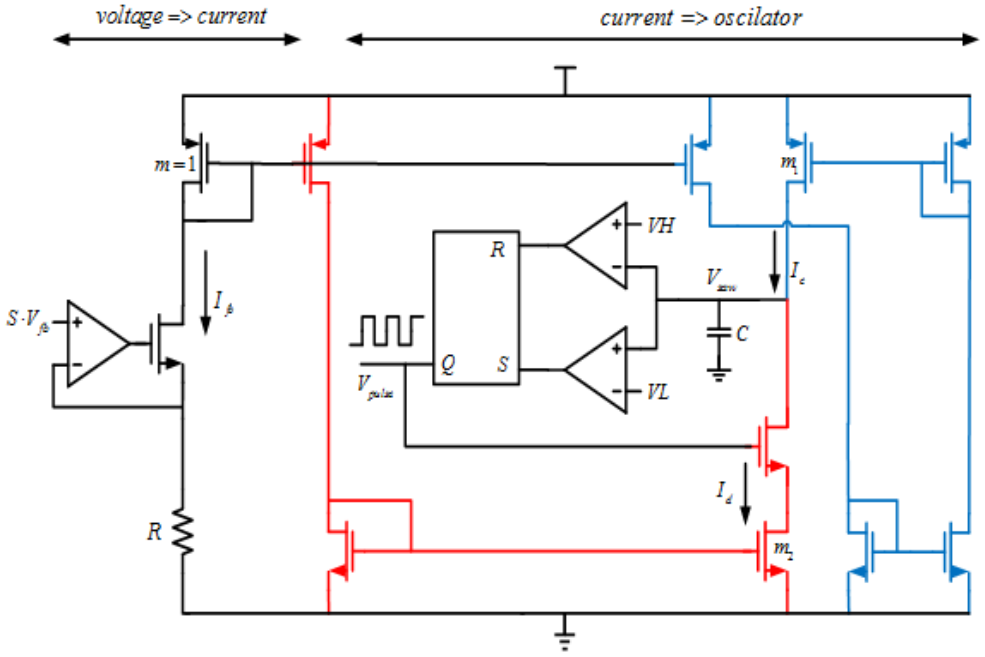

Fig. 5. *Voltage control oscillator for regulating the ratio of frequency to output voltage.*

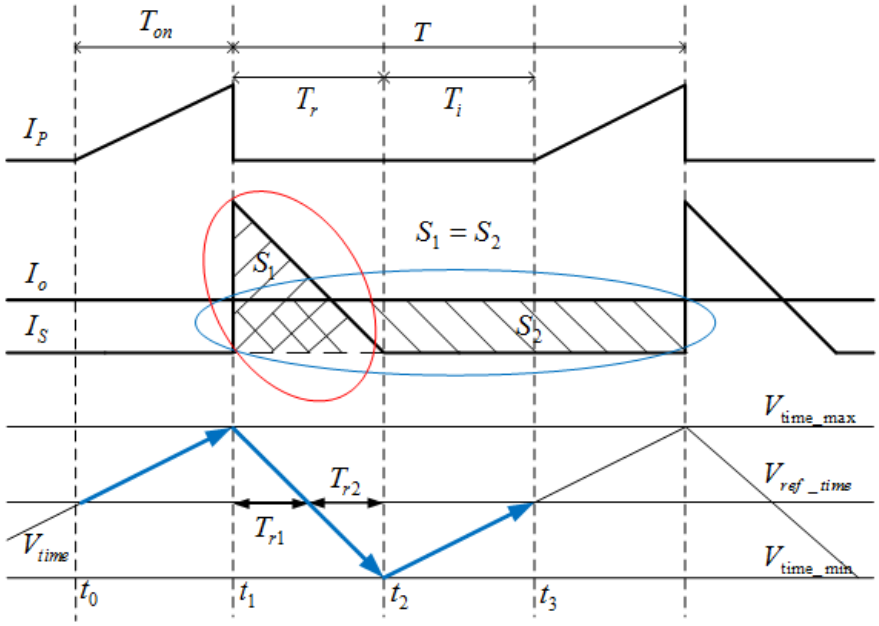

Fig. 6. *Waveforms of DCM fly-back converter primary and secondary current.*

The Voltage-Follower can copy the feedback voltage form auxiliary winding to across the trimming resistor R and achieve the transform from voltage to current.

$$I_{fb} = S \cdot V_{fb} / R \tag{10}$$

And under the acting of the transformer, Vfb can reflect output voltage during secondary winding flows current,

$$V_{fb} = \frac{N_a}{N_s} V_o \tag{11}$$

Accurately,

$$V_{fb} = \frac{N_a}{N_s} V_o - V_{diode}, V_{diode} = 0.7V \tag{12}$$

The varying current with feedback signal will be mirrored into changing and discharging current with different multiplier. $I_c = m_1 I_{fb}, I_d = m_2 I_{fb}$.

Pulse signal is generation through hysteresis control logic with saw voltage signal input.

$$C = Q/U = It/U => t = CU/I \quad (13)$$

The period of each cycle is obtained by

$$T = t_c + t_d = C \cdot \Delta V \cdot (1/I_c + 1/I_d) \quad (14)$$

Where $\Delta V = VH - VL$.

As a result,

$$\frac{1}{f} = (\frac{1}{m_1} + \frac{1}{m_2}) \cdot \frac{VH - VL}{S \cdot V_{fb}/R} \cdot C \quad (15)$$

The ratio of frequency to output voltage can be simplified as,

$$\frac{f}{V_o} = \frac{N_a}{N_s} \cdot \frac{S}{mRC\Delta V} \quad (16)$$

Where $m = 1/m_1 + 1/m_2$.

When the output load is higher than the rated output power point, the output voltage drops and feedback voltage also decreases. The oscillator frequency drops to keep the output current constant. So the output current is independent to supply voltage and load in an ideal condition.

5. PSR with Zero-Cross Detection

The forward-biasing voltage drop on the essential rectifier diode and power lost on auxiliary winding make the foregoing auxiliary winding feedback solution with lower output current accuracy and system efficiency. For a balance between cost and accuracy, an AC-DC converter with zero-cross detection (ZCD) is introduced in this section with principle analysis and schematic design base on DCM fly-back topology. Some of this section works have already been published on [15]. However, a more distinct discussion for the same problem is included in this paper.

A. principle analysis

As depicted in Fig.6, the output current is an average value for the area of S_1 distributed uniformity on the region of S_2 in an entire period T under the influence of filter capacitor.

As the two areas is equal, that is

$$\frac{1}{2} I_{spk} \times T_r = I_o \times T \quad (17)$$

By combining Eq. (2), consequently, output current can be expressed as

$$I_o = \frac{1}{2}(N_p/N_s) \cdot (T_r/T) \cdot I_{ppk} \quad (18)$$

N_p/N_s is depend on the physics structure of the fly-back transformer, and it can be concerned a constant value. A constant output current can be obtained if the primary peak current value and the ratio of interval of secondary winding conducting current to the switching period are both regulated in the proposed design. These can be achieved by the primary-side feedback without auxiliary winding, but using a timing check circuitry to regulate the ratio and a current sense circuit to set the primary peak current value. Based on above discussion, the two decisive factors for constant output drive current is the primary peak current and ratio of duration of secondary side flowing current to period.

The principle and schematic for regulating the primary peak current value is same as section IV. B

B. Regulate ratio of interval of secondary winding conducting current to the switching period

For regulating the ratio of interval of secondary winding conducting current to the switching period, timing checking logic circuit is proposed, as depicted in Fig.6 and Fig.7, based on the work of Weidong Nie et al [13].

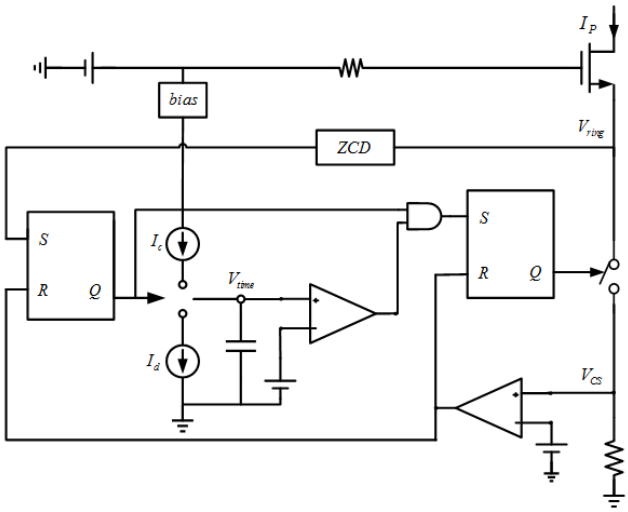

Fig. 7. *Regulate the ratio of interval of secondary winding conducting current to switching period.*

As foregoing discussion, the Current Sense circuit can specify the primary peak current value. So when current sense voltage reaches to the setting reference voltage point, the timing capacitor will be switched to discharging state. The termination of interval of secondary winding conducting is depended on zero-cross detection (ZCD) signal. When the secondary winding current decreases to zero, the drain voltage of power NMOS has a step change and a resonance will occur for RLC circuit consisted by primary inductance, parasitic capacitor of NMOS and gate resistor. Only after timing capacitor is recharged and the voltage across the timing capacitor climbs to reference, a new cycle begin with turning on the primary-side switch, as depicted in Fig.6.

The charging and discharging current for timing capacitor are mirrored from a same current source, $I_c = m_1 I_{bias}$ and $I_d = m_2 I_{bias}$.

The duration of primary side switch turning on time can be expressed as

$$T_{on} = (V_{\text{time\_max}} - V_{ref\_time}) \cdot C_{time}/I_c \quad (19)$$

And the interval of secondary winding conducting current $T_r = T_{r1} + T_{r2}$, where

$$T_{r1} = (V_{\text{time\_max}} - V_{ref\_time}) \cdot C_{time} / I_d \quad (20)$$

$$T_{r2} = (V_{ref\_time} - V_{\text{time\_min}}) \cdot C_{time} / I_d \quad (21)$$

After secondary winding current dropping to zero to the start next cycle, the idle interval can be expressed as

$$T_i = (V_{ref\_time} - V_{\text{time\_min}}) \cdot C_{time} / I_c \quad (22)$$

The period is $T = T_{on} + T_r + T_i$. So the ratio of secondary winding conducting duration T_r to the period T can be obtained as

$$\frac{T_r}{T} = \frac{m_1}{m_1 + m_2} \quad (23)$$

In conclusion, a constant output current can be got with a specified primary peak current I_{ppk} and the ratio of T_r to the period T, and be given by:

$$I_o = \frac{1}{2} \cdot \frac{m_1}{m_1 + m_2} \cdot \frac{N_p}{N_s} \cdot \frac{V_{ref\_CS}}{R_{CS}} \quad (24)$$

C. Zero-cross detection analysis and design

For detecting the time point of secondary winding conduction current dropping to zero, Zero Cross Detection (ZCD) circuitry is elaborated designed. As shown in Fig.8, the important part of ZCD sensing circuit that is the resonant RLC circuit which consists of primary winding inductor L, parasitic capacitors C of power NMOS and gate resistor R.

During Tr, secondary winding conduction current drops linearly from peak value to zero. The drain voltage of power NMOS is

$$V_D = V_{in} + (N_P / N_S) \times V_o \quad (25)$$

After secondary winding current dropping to zero, fly-back transformer will be in high resistor state without current [14]. And the drain voltage of power NMOS lost $(N_P / N_S) \cdot V_o$ immediately. The voltage step variation is reason resonance occurring at the zero crossing point of secondary winding current.

A useful parameter is the damping factor ζ, which is defined as the ratio of α to ω_0,

$$\varsigma = \frac{\alpha}{\omega_0} = \frac{R_G}{2} \sqrt{\frac{C_S}{L_P}} \quad (26)$$

The special case of ζ = 1 is called critical damping and represents the case of a circuit that is just on the border of oscillation. It is the minimum damping that can be applied without causing oscillation. Take this into consideration, the design components parameters should guarantee ζ <1.

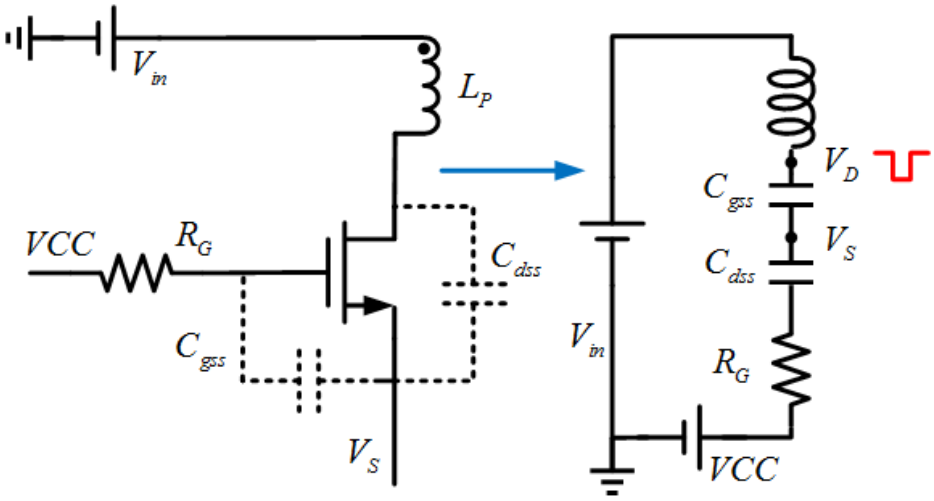

Fig. 8. *Resonance caused by RLC.*

A damped oscillation voltage at drain node of power NMOS can be expressed as [10],

$$\Delta V_D(t) = \frac{N_P}{N_S} \cdot V_o \cdot e^{-\alpha t} \cos(2\pi f_r t) \quad (27)$$

where $\alpha = \frac{R_G}{2L_P}$, $f_r = \frac{1}{2\pi\sqrt{L_P C_d}}$, $\omega_0 = \frac{1}{\sqrt{L_P C_S}}$, $C_S = C_{dss} + C_{gss}$.

So the source voltage experiences a voltage change during resonant period which can be given by

$$\Delta V_S(t) = \left(\frac{-j}{\omega C_{dss}} \| \frac{-j}{\omega C_{gss}} + R_G\right) \cdot \left(\frac{-j}{\omega C_{dss}} + R_G\right) \cdot \Delta V_D(t)$$

Where $\omega = 2\pi f_r$.

If $R_G \ll \left| \frac{-j}{\omega C_{dss}} \| \frac{-j}{\omega C_{gss}} \right|$, $\Delta V_S(t)$ can be simplified as

$$\Delta V_S(t) \approx \frac{-1}{\omega^2 (C_{dss} + C_{gss}) C_{dss}} \cdot \Delta V_D(t) \quad (28)$$

As depicted in Fig. 9, the schematic which consists of two switches and two resistors for setting a proper DC source voltage of power NMOS before resonance occurring by obtunding the decrease before secondary winding conduction current dropping to zero. If without this obtunding circuit, the source voltage drops to an unspecified value after an undefined $(T_r - T_{blank})$.

During ON time, both switch turn off and Vs decrease closed to ground. During blanking time, both switch turn on and Vs increase to near VCC. After that and before secondary winding current dropping to zero, S1 turns on and S2 turns off.

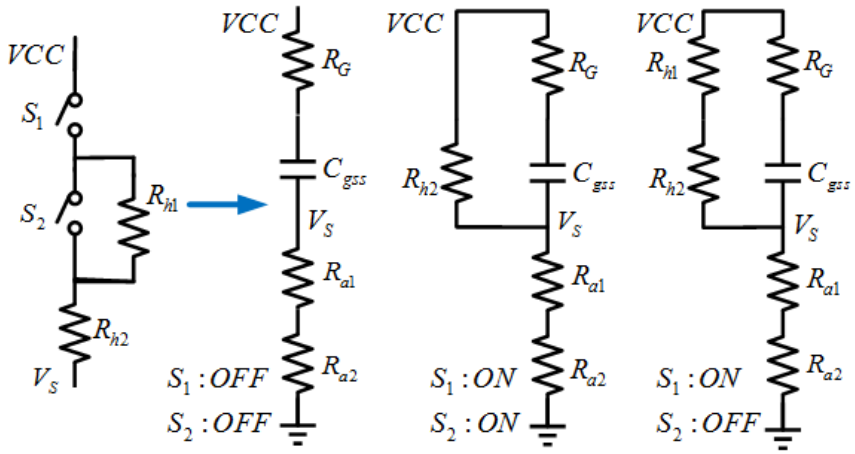

Fig. 9. *Obtunding circuit.*

The decreases of source voltage during $(T_r - T_{blank})$ can be given by,

$$\Delta V_S = \frac{VCC \cdot (R_{h1} + R_{h2})}{R_{a1} + R_{a2} + R_{h1} + R_{h2}} \cdot (1 - e^{-t/\tau}) \qquad (29)$$

Where $\tau = [R_G + (R_{h1} + R_{h2}) \,||\, (R_{a1} + R_{a2})] \cdot C_{gss}$, and $t = T_r - T_{blank}$.

Before secondary winding conduction current dropping to zero, the source voltage of NMOS should be higher than reference voltage. If unfortunately source voltage drop to reference voltage prematurely will cause logic error.

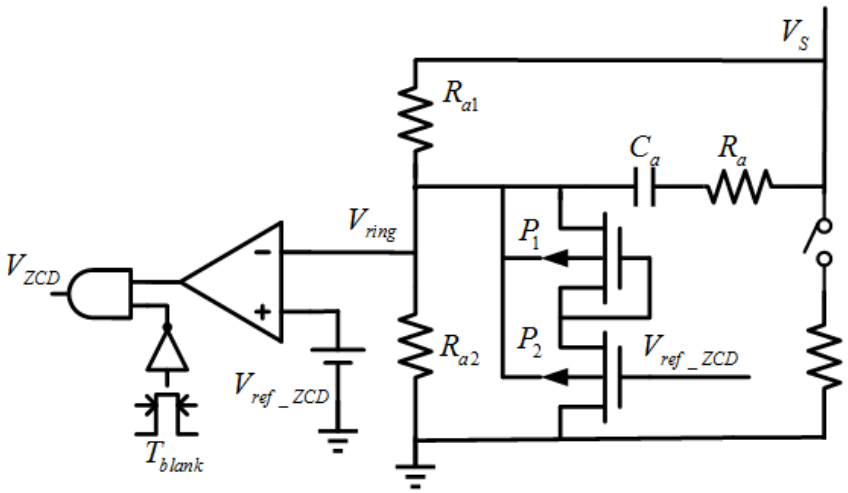

Fig. 10. *Magnify the ring signal for ZCD.*

For taking the input scope of voltage comparator into concerned, the source voltage should be divided into a suitable value for compared with reference voltage for ZCD. Usually, the divided resistors are very larger, even larger enough to over-damp the resonant seriously. At the worst situation, even there is ringing occurring on source of power NMOS, the divided voltage cannot be detected with ring signal and an logic error happened. For avoiding it, the Adjusting circuit for amplifying the ring signal is proposed in the ZCD schematic. It is consisted by a Resonance Magnify RC and Carriers Release PMOS, as depicted in Fig. 10.

As depicted in Fig. 10, the Body of each Release PMOSs is connected to ring voltage but not VCC. After interval ON time, the primary-side switch turns off. Due to the leakage inductance on primary winding and the parasitic capacitance of power NMOS, the ringing occurs. If unfortunately, the ring

is larger enough to be missed consider as ZCD signal, the system will be fail for logic error. A blanking time is set for avoiding ring causing by leakage inductor when primary-side power transforms to secondary-side.

If

$$V_{ring} - V_{ref\_ZCD} > V_{thP} \tag{30}$$

The Release PMOS can be turn on and release the carriers for weaken the unintended lager ringing.

During the ZCD resonant, the RC magnify circuit can deliver the ringing through its RC. A more explicit ZCD can be transformed to the comparator.

By using complex resistor concept, the whole resistors can be expressed as,

$$Z_{all} = R_{a2} + R_{a1} \| (\frac{1}{j\omega C_a} + R_a) \tag{31}$$

The capacitor C_a is used in the Adjust circuit for blocking direct current while allowing alternating current to pass. So the DC part of V_{ring} can be expressed as

$$V_{ring\_DC} = V_{S\_DC} \cdot R_{a2} / (R_{a1} + R_{a2}) \tag{32}$$

And AC part of V_{ring} is depicted follow,

$$V_{ring\_AC} = V_{S\_AC} \cdot R_{a2} / Z_{all} \tag{33}$$

If without the ring magnify capacitor C_a,

$$V_{ring\_AC} = V_{S\_AC} \cdot R_{a2} / (R_{a1} + R_{a2}) \tag{34}$$

For $\left|\frac{R_{a2}}{Z_{all}}\right| > \frac{R_{a2}}{R_{a1} + R_{a2}}$, the Adjusting circuit can magnify the ring from its original version.

6. Simulation and Comparison

The proposed primary-side regulation with auxiliary winding and zero-cross detection converter CMOS IC is implemented in Shanghai Huahong 1um 5V/40V CMOS process. It is used Cadence Spectre to simulate the schematic.

A. PSR with auxiliary winding simulation results

The control logic of primary-side regulation with auxiliary winding is expressed as following. As depicted in Fig.4, 5 and 11 when the voltage across the capacitor Vsaw reaches to reference voltage VH, Vpulse converts from 0 to 1. Vpulse=1 causes Vdrive=0. No matter what state of Vcs, Vpulse=1 can decide independently the operation state with Vdrive=0 and Vcs=0. In other words, Vpulse=1 can reset the logic and prepares for the next new cycle. After that capacitor in Fig.5 will be discharged, when Vsaw drops to reference voltage VL, Vpulse turns to 0, a new cycle stats with primary-side current increasing linearly with slope Vin/Lp. After Ip reaching to Ippk, the switch on the primary-side will be turned off for current sense control.

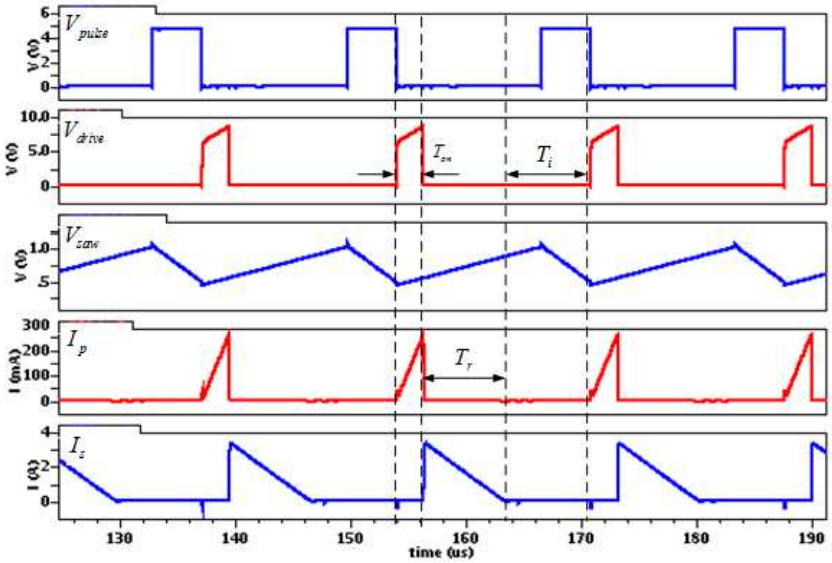

Fig. 11. *PSR with auxiliary winding control logic.*

In other words, the Vpulse can trigger the starting of each cycle and the Vcs can trigger the end of driving pulse. Two things should be taken into consideration that before Vsaw reaches up to VH, Ip must reach to Ippk. Otherwise, Vsaw reaching to VH will reset the state by turning off primary-side switch. And before Vsaw drops down to VL, secondary winding current Is must drop down to zero. Otherwise, Vsaw dropping to zero will start the next new cycle by turning on primary-side switch. And this is also the condition of the system operating in DCM.

In the worst case with the lowest Vin and lowest Vout, means longest Ton and longest Tr. The internal frequency should make sure the system operate DCM at the worst case. It is better has a frequency reduction function to prevent continuous conduction mode by extending the switching period.

The VCO can influence the frequency with various feedback voltages, as depicted in Fig.12. Actually, the changing on VFB pin is hysteretic if output voltage is various. The VFB pin only can reflect the output voltage when secondary winding conducts current. Also the feedback voltage sent to IC is less than VFB for diode forward biasing dropping voltage, about 0.7V. There is a capacitor on VFB and ground, also a resistors divided network. Capacitor can hold the feedback voltage and resistors can refresh. A variation load with higher voltage can be reflected to feedback voltage immediately. A changing load with lower voltage only can be reflected on auxiliary after 0.5s for refresh VFB. Because rectifier diode on auxiliary-side is reverse-biasing during this 0.5s before hold capacitor fully discharge.

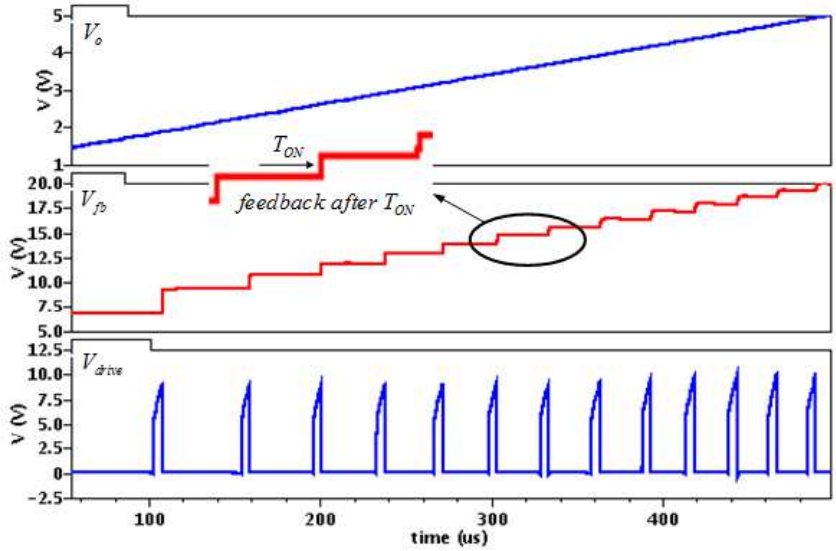

Fig. 12. *Load voltage line changing simulation result.*

B. PSR with zero-cross detection simultion results

As depicted in Fig.13, firstly, the primary-side current reaches to peak value with slope Vin/Lp during ON time. And also timing capacitor is charged form reference voltage to peak value. When primary-side switch turns off, the power stored on primary winding will be transformed to secondary winding. The rectifier diode current decreases from peak value to zero with slope Vo/Ls. It must be guaranteed that the voltage across the timing capacitor in Fig.7 decreases under the reference voltage during Tr. The termination of interval of secondary winding conducting is detected with zero-cross detection (ZCD) and triggers change timing capacitor again. Only after timing capacitor is recharged and the voltage across the timing capacitor climbs to reference voltage, a new cycle is allowed to begin with turning on the primary-side switch. In this proposed design, the multiplier of charging and discharging current to biasing current is same. So Ton=Tr1 and Ti=Tr2. The ratio of interval of secondary winding conducting current to switching period is set on 0.5. Under this regulation, the idle time can be adaptive according various load conditions.

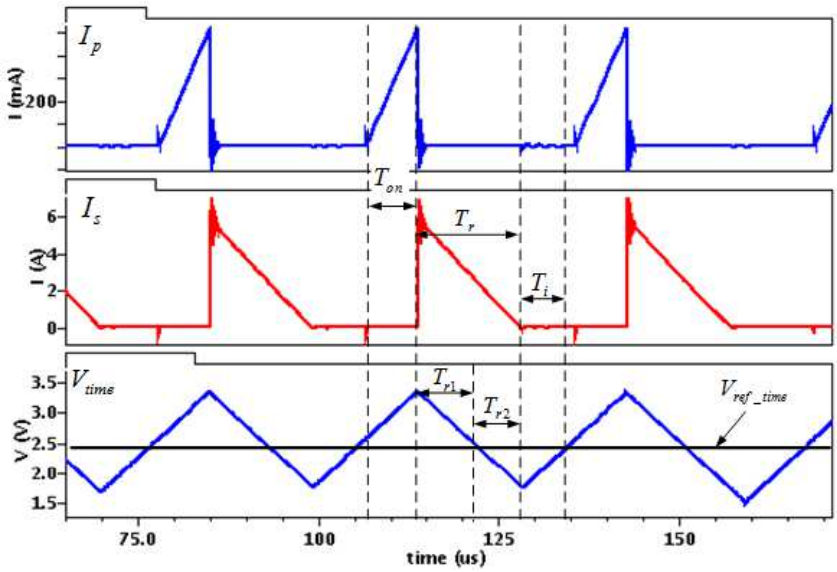

Fig. 13. *PSR with ZCD timing check simulation.*

When resonant occurs, the RC magnify circuit in Fig.10 can amplify the ringing through its RC. A more explicit ring signal can be transformed to the voltage comparator for ZCD. As depicted in Fig.14, due to leaking inductance on primary winding, a resonance occurs when primary-side switch converting from turning on to turning off. This ring signal can be wrong regarded as zero cross point. A blanking time has been set to eliminate this influence.

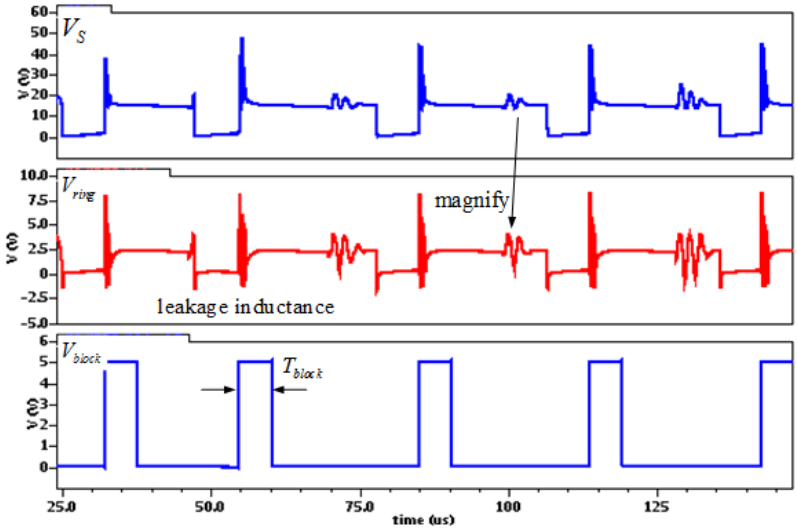

Fig. 14. *Magnify ring and block ring causing by leakage inductance.*

C. comparison

No matter secondary-side regulation with opto-coupler or primary-side regulation with auxiliary winding or with zero-cross detection, both of them are widely used in today electronic applications. A brief compare is given in Table.1.

Table 1. *Compare between SSR and PSR.*

Items	SSR with opto-coupler	PSR with Auxiliary	PSR with ZCD
Accuracy	1%-3%	10%	5%
Efficiency	75%-80%	82%	85%
System Cost	expensive	middle	cheap
Design Complexity	middle	easy	complex

By using the opto-coupler for isolation, the feedback circuitry can be placed on the secondary-side. So the output load condition can be directly sensed and regulated. It is an advantage for SSR with opto-coupler and has fast feedback response for better output current accuracy. However, if the system size is strictly limited, the large volume of opto-coupler becomes a major problem for PCB design. Also, the use of photoelectric coupler and precision voltage source cased insecurity isolation between primary side and secondary side. An opto-coupler introduces an extra pole in the control loop for its large parasitic capacitance, which reduces the converter's bandwidth and more hard to compensate the control loop.

Contrary to SSR with opto-coupler, the PSR with auxiliary winding has lower cost and smaller volume. The IC and PCB circuitry is simpler. However, the forward biasing voltage across the rectifier diode can influence the accuracy of a PSR with auxiliary winding. Actually, the changing on VFB pin is hysteretic if output voltage is various. The VFB pin only can reflect the output voltage when secondary winding conducts current.

Without power lost on opto-coupler or auxiliary winding, PSR with ZCD has the higher efficiency. Also eliminate the using the expensive opto-coupler and complex three windings transformer, PSR with ZCD design system is cheap with less outside PCB circuitry. However, timing check control is more sensitive to fabricate process variation and temperature influence. Temperature variations have an adverse effect on tolerance. This can be mitigated by introducing a resistor with opposing temperature coefficient (TC) to threshold voltage.

7. Conclusion

For a balance between system production cost and output regulation accuracy, an AC-DC converter with zero-cross detection (ZCD) and magnifying ring signal function is proposed in this paper. Control principle analysis and comparison on accuracy, efficiency and cost between the SSR with opto-coupler, PSR with auxiliary winding and PSR with ZCD solutions are given in this paper for a brief summarizing AC-DC converter with constant current output CMOS IC design based on discontinuous conduction mode (DCM) fly-back topology.

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